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L7 and (plurality near2 wires)	2

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DATE: Monday, March 17, 2003 Printable Copy Create Case

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	DB=USPT; PLUR=YES; OP=ADJ		
L8	L7 and (plurality near2 wires)	2	L8
L7	L6 and (plate or plates)	73	L7
L6	L1 and (elongated adj (opening or via or hole or contact))	118	L6
L5	L3 and (elongated near2 (opening or hole or via))	5	L5
L4	L3 and (plurality near3 electrodes)	5	L4
L3	L2 and (upper near plate)	131	L3
L2	L1 and (lower near plate)	230	L2
L1	semiconductor adj chip	25412	L1

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1. Document ID: US 5307503 A

L8: Entry 1 of 2 File: USPT Apr 26, 1994

US-PAT-NO: 5307503
DOCUMENT-IDENTIFIER: US 5307503 A

TITLE: Shielded circuit module with terminal pins arrayed on four sides for connection to a computer board

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

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2. Document ID: US 4762267 A

L8: Entry 2 of 2 File: USPT Aug 9, 1988

US-PAT-NO: 4762267
DOCUMENT-IDENTIFIER: US 4762267 A

TITLE: Wire bonding method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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Terms	Documents
L7 and (plurality near2 wires)	2

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L8: Entry 1 of 2 File: USPT Apr 26, 1994

DOCUMENT-IDENTIFIER: US 5307503 A
TITLE: Shielded circuit module with terminal pins arrayed on four sides for connection to a computer board

Brief Summary Text (8):
FIGS. 3 and 4 show the first POACH 12. The first POACH 12 has a stage 100, a plurality of leads 101, a semiconductor chip 102, a plurality of wires bonded to connect chip 102 and the leads 101, and a synthetic resin-formed package portion 104. Each lead 101 has a shape such that the inner end thereof is narrow and the outer end thereof is wide. A length L.sub.2 of each lead 101 is about 8 mm which is approximately four times a length L.sub.1 of the wire 103 which is about 2 mm. For this reason, the size of the first POACH 12 is 29 mm.times.29 mm which is relatively large. A thickness t.sub.1 of the first POACH 12 is 3.9 mm.

Drawing Description Text (10):
FIG. 9 is a perspective view for explaining a relationship of a pin terminal assembly of the computer module and an elongated opening of the case;

Detailed Description Text (13):
As shown in FIGS. 7 and 8, the computer module 30 is accommodated within a case 82 and is shielded in a state where only the pin terminals 58 project from the case 82. The case 82 is made up of a metal case portion 80 and a lid portion 81. As shown in FIG. 9, elongated openings 84 are provided along the four sides of a bottom plate portion 83 of the case portion 80. As may be seen from FIGS. 7, 8 and 9, the pin terminals 58 project from the peripheral portion of the bottom surface of the case 82 through the elongated openings 84.

Detailed Description Text (27):
The POACH 33 has a stage 100, a semiconductor chip 102 bonded on the stage 100, a plurality of leads 111, wires 112 bonded to pads on the semiconductor chip 102 and tips of the leads 111, and a synthetic resin-formed package portion 113. A length L.sub.3 of the wire 112 is determined by the specifications of a wire bonder, and is about 2 mm which is a normal value for a common semiconductor device. A length L.sub.4 of the lead 111 is about 2 mm which is approximately the same as the length L.sub.3 of the wire 112. For this reason, the size a.sub.2 .times.b.sub.2 of the POACH 33 is 14 mm--14 mm which is reduced to approximately 1/4 the POACH 12 of the prior art.

Detailed Description Text (28):
If FIG. 12 is reduced to a size such that the semiconductor chip 102 shown in FIG. 12 becomes the same size as the semiconductor chip 102 shown in FIG. 3, it will be understood from a comparison with FIG. 3 that the size of the POACH 33 is considerably smaller than that of the POACH 12 of the prior art. A thickness t.sub.2 of the POACH 33 is 2.5 mm which is thinner than the POACH 12 of the prior art. The lead 111 has a shape such that a width thereof is approximately the same over the total length of the lead 111. A width w.sub.1 of the lead 111 is 0.18 mm.

Detailed Description Text (33):
Next, a description will be given of the stage 110. The size of the stage 110 is approximately the same as that of the semiconductor chip 102. At several parts along an outer periphery of the stage 110, there are provided extension portions 115-1 through 115-5 which extend from the stage 110 in a U-shape and form openings therein. Among the pads on the semiconductor chip 102, a pad 116 to be grounded is bonded to a wire 112-1 and is grounded by way of the wire 112-1 and the U-shaped extension portion 115-1. A lead 111-5 to be grounded is connected to the U-shape extension portion 115-2 through a wire 112-2. By providing the U-shaped extension portions 115-1 through 115-5, the size of the stage 110 is reduced to a minimum size which is substantially the same as that of the semiconductor chip 102. For this reason, the thermal distortion due to a difference in the coefficients of thermal expansion of the package portion 113 and the stage 110 is suppressed to a minimum, and the adverse influence of the thermal distortion is thereby suppressed.

CLAIMS:

1. A circuit module connectable to a board in a computer comprising:

at least one semiconductor part;

a substrate having a rectangular shape, said semiconductor part being mounted on said substrate;

terminals arranged on an outer periphery of said substrate along four sides of said substrate;

a case, having a case portion and a lid portion, for accommodating and shielding said substrate, one of said case portion and said lid portion having elongated openings for exposing said terminals; and wherein:

said semiconductor part includes a central processing unit, a memory circuit part, and a control circuit part, said semiconductor part being mounted on at least one of top and bottom surfaces of said substrate;

said semiconductor part includes a semiconductor chip, leads arranged radially around said semiconductor chip, wires connecting said semiconductor chip and said leads, and a synthetic resin package portion for sealing said semiconductor chip, said leads and

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L5	L3 and (elongated near2 (opening or hole or via))	5	L5
L4	L3 and (plurality near3 electrodes)	5	L4
L3	L2 and (upper near plate)	131	L3
L2	L1 and (lower near plate)	230	L2
L1	semiconductor adj chip	25412	L1

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1. Document ID: US 6333206 B1

L4: Entry 1 of 5 File: USPT Dec 25, 2001

US-PAT-NO: 6333206
DOCUMENT-IDENTIFIER: US 6333206 B1

TITLE: Process for the production of semiconductor device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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2. Document ID: US 6175159 B1

L4: Entry 2 of 5 File: USPT Jan 16, 2001

US-PAT-NO: 6175159
DOCUMENT-IDENTIFIER: US 6175159 B1

TITLE: Semiconductor package

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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3. Document ID: US 5757075 A

L4: Entry 3 of 5 File: USPT May 26, 1998

US-PAT-NO: 5757075
DOCUMENT-IDENTIFIER: US 5757075 A

TITLE: Semiconductor heat sink apparatus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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4. Document ID: US 5677569 A

L4: Entry 4 of 5 File: USPT Oct 14, 1997

US-PAT-NO: 5677569
DOCUMENT-IDENTIFIER: US 5677569 A

TITLE: Semiconductor multi-package stack

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

5. Document ID: US 4376983 A

L4: Entry 5 of 5 File: USPT Mar 15, 1983

US-PAT-NO: 4376983
DOCUMENT-IDENTIFIER: US 4376983 A

TITLE: High density dynamic memory cell

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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Terms	Documents
L3 and (plurality near3 electrodes)	5

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L4: Entry 1 of 5 File: USPT Dec 25, 2001

DOCUMENT-IDENTIFIER: US 6333206 B1
TITLE: Process for the production of semiconductor device

Abstract Text (1):
The present invention provides a process for the production of a semiconductor device comprising a semiconductor element provided on a printed circuit board with a plurality of connecting electrode portions provided interposed therebetween, the gap between said printed circuit board and said semiconductor element being sealed with an underfill resin layer. In accordance with the present invention, (1) the underfill resin layer is formed by melting a lamellar solid resin provided interposed between said printed circuit board and said semiconductor element, and (2) the lamellar solid resin provided interposed between said printed circuit board and said semiconductor element is heated for a predetermined period of time until the temperature of the solid resin layer reaches a predetermined range where the two components are connected to each other under pressure under the following conditions (X) and (Y): (X) Supposing that the initial residual heat of reaction of the solid resin before heating is 100% as determined by a differential scanning calorimeter (DSC), the residual heat of reaction thereof is not more than 70% of the initial residual heat of reaction; and (Y) The temperature of the semiconductor element is predetermined higher than that of the printed circuit board, and the difference in temperature between them is not less than 50.degree. C. In this manner, a production process which facilitates the resin sealing of the gap between the semiconductor element and the board and thus can inhibit warpage of the entire semiconductor device and a semiconductor device having an excellent reliability can be provided. In the present invention, the use of a sheet-like underfill material which gives an underfill resin layer having an elastic modulus in tension at 25.degree. C. of from 300 to 15,000 MPa when hardened can provide a semiconductor device which exerts an excellent effect of relaxing the stress on the semiconductor element, printed circuit board and connecting electrode portions and thus exhibits a high reliability.

Brief Summary Text (8):
In order to accomplish the foregoing object of the present invention, the first aspect of the process for the production of a semiconductor device according to the present application comprises mounting a semiconductor element on a printed circuit board with a plurality of connecting electrode portions provided interposed therebetween, and then sealing the gap between the foregoing printed circuit board and semiconductor element with an underfill

resin layer, characterized in that said underfill resin layer is formed by melting a lamellar solid resin provided interposed between the foregoing printed circuit board and semiconductor element.

Brief Summary Text (9):
In other words, the present invention comprises sealing with an underfill resin layer the gap between a printed circuit board and a semiconductor element which have been connected to each other with a plurality of connecting electrode portions provided interposed therebetween to produce a semiconductor device, characterized in that said sealing resin layer is formed by melting and hardening a lamellar solid resin provided interposed between the foregoing printed circuit board and semiconductor element. Thus, the connection between the foregoing printed circuit board and semiconductor element is completed while melting the foregoing lamellar solid resin, preferably under pressure. Accordingly, as compared with the conventional complicated process which comprises connecting a printed circuit board to a semiconductor element, and then injecting a sealing resin into the gap therebetween to complete the connection, the connection between the foregoing printed circuit board and semiconductor element and the sealing the gap therebetween with a resin can be effected at a time, drastically simplifying the production process. Further, since a solid resin having excellent storage properties is used as a sealing resin instead of liquid resin, the production process is not liable to the foregoing various problems caused by the injection of the liquid resin into the gap.

Brief Summary Text (13):
In addition, the underfill resin layer formed by melting the foregoing solid resin can be easily formed by a process which comprises providing an underfill resin layer on one side of the foregoing semiconductor element, placing the semiconductor element on a printed circuit board having a plurality of connecting electrode portions provided thereon in such an arrangement that the underfill resin layer comes in contact with the connecting electrode portions, heating and melting the foregoing underfill resin layer so that the underfill resin thus molten is packed into the gap between the printed circuit board and the semiconductor element, and then hardening the underfill resin. Alternatively, the underfill resin layer formed by melting the foregoing solid resin can be easily formed by a process which comprises providing an underfill resin layer on one side of the foregoing printed circuit board, placing a semiconductor element having a plurality of connecting electrode portions provided thereon on the printed circuit board in such an arrangement that the connecting electrode portions thereof come in contact with the underfill resin layer, heating and melting the foregoing underfill resin layer so that the underfill resin thus molten is packed into the gap between the printed circuit board and the semiconductor element, and then hardening the underfill resin.

Detailed Description Text (4):
The semiconductor device produced by the process for the production of a semiconductor device according to the present invention is configured such that a semiconductor element 3 is mounted on one

side of a printed circuit board 1 with a plurality of connecting electrodes 2 provided interposed therebetween as shown in FIG. 1. Further, an underfill resin layer 4 is formed between the printed circuit board 1 and the semiconductor element 3.

Detailed Description Text (6):
Accordingly, in a normal embodiment, the plurality of connecting electrode portions 2 for electrically connecting the printed circuit board 1 to the semiconductor element 3 may have a joint ball or the like provided on the surface of either or both of the printed circuit board 1 and the semiconductor element 3. Both the two electrode portions may be made of an electrode alone.

Detailed Description Text (7):
The material constituting the plurality of connecting electrode portions (joint balls) 2 is not specifically limited. In practice, however, a gold stud bump, a low melting temperature solder bump, so-called eutectic solder bump, a high melting point solder bump, a gold-plated bump with a copper or nickel core, etc. may be used. The lamellar solid resin according to the present invention may be used also for the purpose of controlling the height of the connecting electrode portions 2 made of the foregoing eutectic solder or a solder material which deforms at a predetermined temperature.

Detailed Description Text (23):
As previously mentioned, the process for the production of a semiconductor device according to the present invention comprises mounting a semiconductor element on a printed circuit board with a plurality of connecting electrode portions provided interposed therebetween, and then sealing the gap between the printed circuit board and the semiconductor element with an underfill resin layer, characterized in that said underfill resin layer is formed by melting a lamellar solid resin provided interposed between the printed circuit board and the semiconductor element. The foregoing process for the production of a semiconductor device can be roughly divided into three embodiments.

Detailed Description Text (25):
As shown in FIG. 2, a solid underfill resin sheet 10 is placed on a printed circuit board 1 having a plurality of spherical connecting electrode portions (joint balls) 2 provided thereon with the connecting electrode portions 2 provided interposed therebetween. Subsequently, as shown in FIG. 3, a semiconductor element 3 is placed on the underfill resin sheet 10 in a predetermined position. The semiconductor element 3 is then tentatively bonded to the underfill resin sheet 10 optionally by making the use of tack. The underfill resin sheet 10 is then heated and melted under pressure so that it is packed into the gap between the semiconductor element 3 and the printed circuit board 1. The underfill resin sheet thus molten is then hardened to seal the gap. Thus, an underfill resin layer 4 is formed. In order to tackify the underfill resin sheet, a rubber component such as acrylonitrile-butadiene copolymer is incorporated in the epoxy resin composition used. In this manner, a semiconductor device shown in FIG. 1 is produced. In accordance with the foregoing pressing procedure, the joint balls 2 are pressed so that they are normally flattened (reduced in height) to

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1. Document ID: US 6366462 B1

L5: Entry 1 of 5 File: USPT Apr 2, 2002

US-PAT-NO: 6366462
DOCUMENT-IDENTIFIER: US 6366462 B1

TITLE: Electronic module with integral refrigerant evaporator assembly and control system therefore

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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2. Document ID: US 6080048 A

L5: Entry 2 of 5 File: USPT Jun 27, 2000

US-PAT-NO: 6080048
DOCUMENT-IDENTIFIER: US 6080048 A

TITLE: Polishing machine

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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3. Document ID: US 4689866 A

L5: Entry 3 of 5 File: USPT Sep 1, 1987

US-PAT-NO: 4689866
DOCUMENT-IDENTIFIER: US 4689866 A

TITLE: Methods for transferring spring clips

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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4. Document ID: US 4674166 A

L5: Entry 4 of 5 File: USPT Jun 23, 1987

US-PAT-NO: 4674166
DOCUMENT-IDENTIFIER: US 4674166 A

TITLE: Spring clip transfer apparatus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw Desc | Image

☐ 5. Document ID: US 4582245 A

L5: Entry 5 of 5 File: USPT Apr 15, 1986

US-PAT-NO: 4582245
DOCUMENT-IDENTIFIER: US 4582245 A

TITLE: Method and apparatus for automated spring clip insertion and removal

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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Terms	Documents
L3 and (elongated near2 (opening or hole or via))	5

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L5: Entry 1 of 5 File: USPT Apr 2, 2002

DOCUMENT-IDENTIFIER: US 6366462 B1
TITLE: Electronic module with integral refrigerant evaporator assembly and control system therefore

Abstract Text (1):
An electronic module is provided having an integrated refrigerant evaporator assembly coupled to a closed-cycle cooling system, as well as a method for controlling the system. The module and integrated assembly includes a plurality of integrated circuit chips arrayed on a substrate. The evaporator assembly is disposed over the chips and substrate such that a chamber is formed between the assembly and the substrate within which the chips reside. A lower plate of the assembly has a plurality of jet orifices which direct coolant onto individual chips of the plurality of chips arrayed on the substrate. In addition, the lower plate includes a plurality of channels formed between at least some of the jet orifices. The plurality of channels remove coolant from the chamber after the coolant has been heated by impinging upon the integrated circuit chips. A control system is provided to prevent excessive pressure from building up within the assembly at startup and shutdown of the closed-cycle cooling system.

Brief Summary Text (7):
Briefly summarized, in one aspect the present invention comprises an electronic module and integrated refrigerant evaporator assembly which includes a plurality of heat generating electronic components arrayed on a substrate. The evaporator assembly is disposed over the electronic components such that the electronic components reside in a chamber between the substrate and the refrigerant evaporator assembly. The refrigerant evaporator assembly is configured to direct coolant onto the plurality of heat generating electronic components, which may comprise integrated circuit chips. More particularly, the evaporator assembly includes a lower plate which has a plurality of jet orifices that are arrayed to direct coolant onto the plurality of heat generating electronic components. The lower plate further includes a plurality of channels formed between at least some of the plurality of jet orifices. The plurality of channels are designed to remove coolant from the chamber after the coolant is heated by the plurality of heat generating electronic components.

Brief Summary Text (10):
To restate, provided herein is an electronic module having an integrated jet impingement refrigerant evaporator assembly, as well as a control method therefor. Advantageously, the electronic module

with integrated evaporator proposed herein is compact and has a low profile. Furthermore, since heat transfer takes place directly between a refrigerant and the semiconductor chips of the module, the evaporator can be made of lightweight, low thermal conductivity materials such as hard plastics. Materials of this type have low thermal capacitance which minimizes initial cool-down time, plus the low thermal conductivity helps to reduce parasitic heat load inherent in low temperature systems. In addition, since tolerances (with the exception of the jet orifices) are not as critical as those of today's module hardware, the cost of producing the evaporator should be relatively low. Subsections may even be molded or pressed (e.g., stamped) with minimal finishing or machining required.

Drawing Description Text (5):
FIG. 2A is a plan view of one embodiment of a lower plate in accordance with the principles of the present invention for the evaporator assembly depicted in FIG. 1B;

Drawing Description Text (6):
FIG. 2B is a cross-sectional elevational view of the lower plate of FIG. 2A taken along line 2B--2B;

Drawing Description Text (9):
FIG. 4A is a plan view of one embodiment of an upper plate in accordance with the principles of the present invention for the evaporator assembly of FIG. 1B;

Drawing Description Text (10):
FIG. 4B is a cross-sectional elevational view of the upper plate of FIG. 4A taken along line 4B--4B;

Detailed Description Text (3):
In this embodiment, a chamber 17 is formed between evaporator assembly 12, disposed over the plurality of integrated circuit chips 16, and substrate 14. Coolant is fed into chamber 17 through a plurality of jet orifices 45 formed in a lower plate 20 of assembly 12. The jet orifices, various embodiments of which are described further below, are disposed in plate 20 in order to impinge coolant directly onto semiconductor chips 16. The coolant is received through an inlet plenum 40 fed through one or more inlet ports 41.

Detailed Description Text (4):
Heated coolant (e.g., gaseous coolant) is advantageously removed from chamber 17 through a plurality of channels 50 formed in lower plate 20 and extending to a perimeter of the array of integrated circuit chips 16 disposed on the substrate. At the perimeter, one or more openings are formed in lower plate 20, an intermediate plate 22 and an upper plate 24 of assembly 12 which are aligned to form one or more outlet channels feeding heated coolant back to an outlet plenum 42, which is in communication with one or more outlets 43. In this embodiment, inlet plenum 40 is defined between lower plate 20 and intermediate plate 22, while outlet plenum 42 resides between intermediate plate 22 and upper plate 24. FIGS. 2A-4B depict one example of plates 20, 22 & 24 in greater detail. However, those skilled in the art will note that various other

configurations can be readily conceived for the plates comprising the evaporator assembly. Further, if desired, the evaporator assembly could be fabricated as a unitary structure having the particular characteristics of the multiplate assembly of FIG. 1B.

Detailed Description Text (5):
In FIGS. 2A & 2B, one embodiment of lower plate 20 is shown. Lower plate 20 again includes a plurality of openings 26 along its periphery which are used to mechanically connect the assembly and the substrate. In this embodiment, plate 20 is provided with multiple 3.times.3 arrays of jet orifices 45 which are assumed to be positioned to align over respective integrated circuit chips disposed on the substrate. Holes are formed/machined in the wells of the inlet plenum to serve as the jet orifices for the refrigerant. The diameter and number of orifices 45 are chosen to optimize cooling requirements. Wells are principally provided to allow for channels 50 that allow the effluent to readily pass to the outer perimeter of the module.

Detailed Description Text (6):
Although shown in FIG. 2A as multiple 3.times.3 arrays, those skilled in the art will note that various combinations of jet orifices could be provided within lower plate 20. For example, if an array of integrated circuit chips disposed on a substrate comprise chips of different heat generating capacity, then additional coolant can be directed onto chips generating greater heat, while integrated circuit chips requiring less cooling can have less jet orifices arrayed over them. Thus, it is conceivable that certain integrated circuit chips may have a 3.times.3 array over them, while other integrated circuit chips may have a 2.times.2 array, or even just one or no jet orifice aligned over them. Again, this invention encompasses the concept that the individual heat generating capacity of each integrated circuit chip on a substrate be considered in configuring the jet orifices of lower plate 20. If certain chips require additional cooling, then a larger number of jet orifices are provided to align over those chips. Also, the 5.times.5 sets of 3.times.3 arrays of jet orifices of FIG. 2A is provided by way of example only, and in practice would be dependent upon the actual array of integrated circuit chips or other heat generating components disposed on the substrate.

Detailed Description Text (7):
Also shown in FIGS. 2A & 2B are channels 50 in the lower surface of plate 20 which facilitate removal of heated coolant to elongated openings 52 disposed at the periphery of the array of integrated circuit chips (see FIG. 1B). These elongated openings 52 align with similar openings in intermediate plate 22 to form an outlet channel for heated coolant to be removed to outlet plenum 42 (FIG. 1B). An x-y pattern of channels 50 is formed in lower plate 20 in between the regions of 3.times.3 jet orifices to facilitate removal of heated coolant to a closest outlet opening 52. The size and shape of channels 50 can vary depending upon the particular array of integrated circuit chips over which the refrigerant evaporator assembly is to be placed.

Detailed Description Text (8):

FIGS. 3A & 3B depict one embodiment of intermediate plate 22. Plate 22 is configured to stack atop lower plate 20 (see FIGS. 2A & 2B) and has inlet ports 41 to the inlet plenum 40 formed between lower plate 20 and intermediate plate 22 (see FIG. 1B). In addition, intermediate plate 22 includes elongated openings 52' which align over elongated openings 52 in lower plate 20 to form the outlet channels. The plurality of openings 26 are disposed along a perimeter of plate 22 to facilitate mechanical connection of the evaporator assembly to the substrate.

Detailed Description Text (9):
FIGS. 4A & 4B depict one embodiment of upper plate 24 of evaporator assembly 12 (see FIG. 1B). Upper plate 24 includes two inlet ports 41 and two outlet ports 43. Two inlet and outlet ports are provided so that continuous operational redundancy associated with today's module refrigeration unit cooling systems can be maintained. Inlets 41 are in communication with inlet plenum 40 of FIG. 1B, while outlets 43 are in communication with outlet plenum 42 of FIG. 1B. A plurality of holes 26 are disposed at the perimeter of upper plate 24 to facilitate mechanical coupling of the assembly to the substrate as noted above. Outlet plenum 42 is defined between intermediate plate 22 and upper plate 24 as shown in FIG. 1B.

Detailed Description Text (10):
In one embodiment, the coolant employed in the assembly comprises a refrigerant. Refrigerants commonly used in medium (down to -40.degree. C.) and low (down to -100.degree. C.) temperature applications are chemically inert dielectric fluids suitable for direct contact with materials typically used in packaged integrated circuit chips today. It is therefore proposed herein to impinge the refrigerant directly onto the integrated circuit chips (for example, processor chips), using the integrated evaporator assembly of FIG. 1B. The substrate carrying the semiconductor chips to be cooled is sandwiched between a base plate and the jet impingement evaporator in a same manner as the substrate is today sandwiched between a base plate and a thermally conducting hat.

Detailed Description Text (11):
In operation, refrigerant enters the evaporator assembly and distributes itself within the inlet plenum and then passes through the jet orifices where it impinges on the semiconductor chips, thus cooling the chips. The effluent makes its way through the channels to the outer perimeter of the substrate and then upward through the four effluent slots to the outlet plenum, and then exits through the outlet ports. In one embodiment, the refrigerant comprises a liquid when introduced through the jet orifices and undergoes heating to become a gaseous-coolant after impinging upon the semiconductor chips. The gaseous-coolant is then removed through the plurality of channels 50 (see FIG. 1B) formed in the lower plate of the assembly.

Detailed Description Text (12):
FIGS. 5A & 5B depict an alternate embodiment of an electronic module 10' employing an evaporator assembly 12 in accordance with the principles of the present invention. Module 10' again includes a substrate 14 upon which one or more integrated circuit chips 16 are arrayed. As shown in the enlargement of FIG. 5B, thermal